

Multicore Computer Architecture - Storage and Interconnects

Lecture 14

Network On Chip Router Micro-architecture



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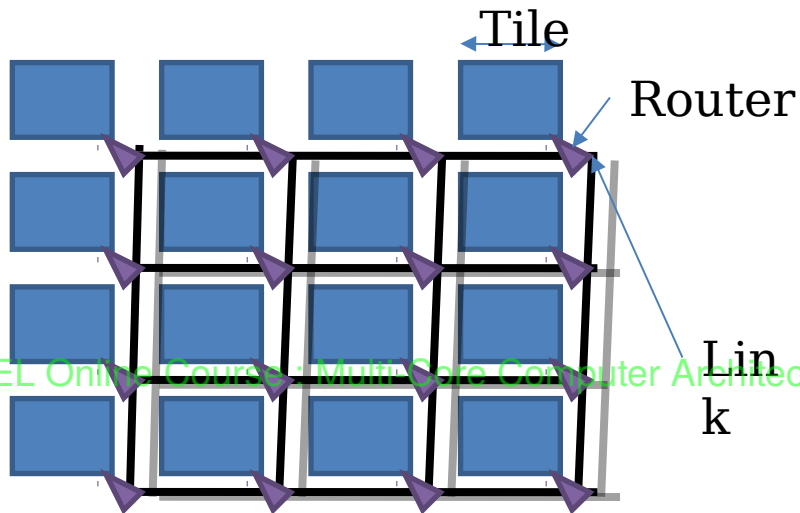
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Building Blocks of NoC



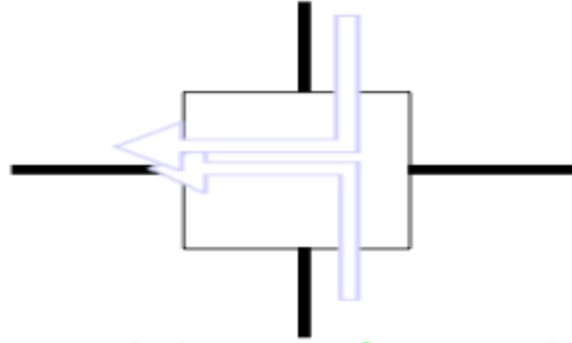
❖ **Topology**

❖ **Routing**

❖ **Flow control**

❖ **Router micro-architecture**

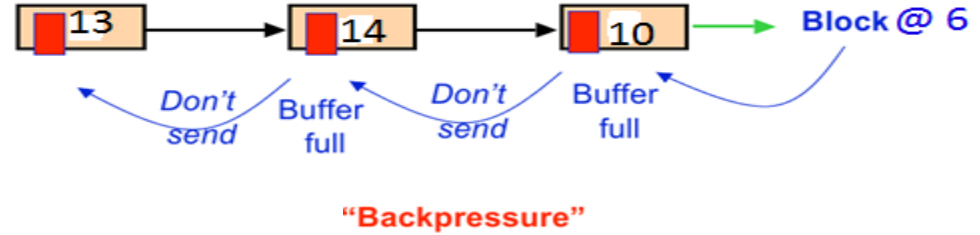
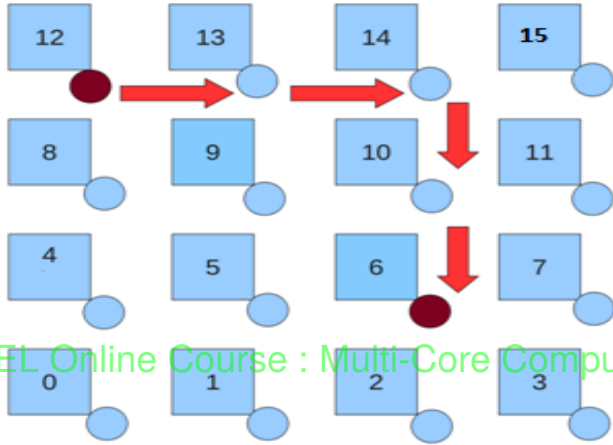
Handling Contention



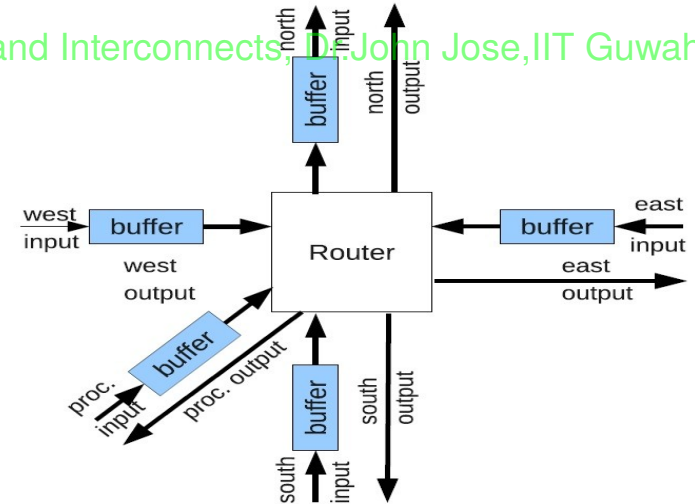
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- ❖ When two packets trying to use the same link at the same time ?
 - ❖ Buffer one (widely used mechanism)
 - ❖ Drop one
 - ❖ Misroute one (deflection)

Flow Control

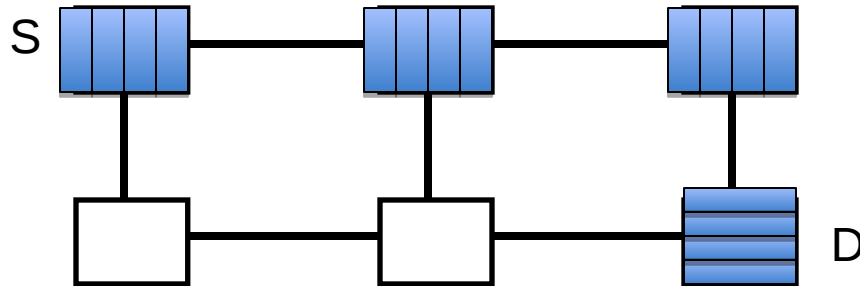


- ❖ Upstream router should know the buffer availability of downstream router.
- ❖ Credit should be exchanged between routers by handshake signals



Store and Forward Flow Control

- ❖ Store and Forward Packet based flow control
 - ❖ Packet copied entirely into network router before moving to the next node
 - ❖ Flow control unit is the entire packet
- ❖ Leads to high per-packet latency
- ❖ Requires buffering for entire packet in each node

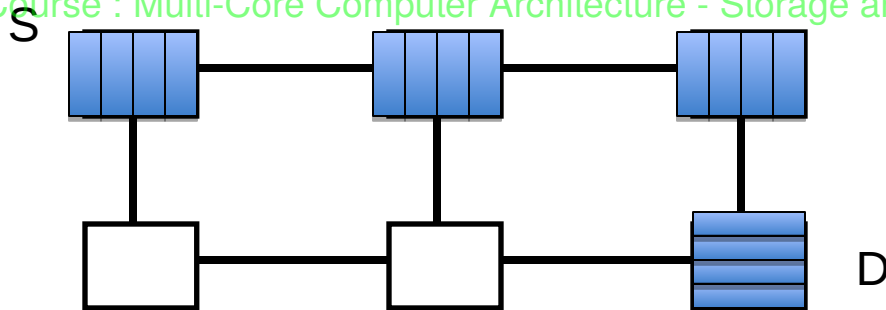


Can we do better?

Cut through Flow Control

- ❖ Another form of packet based flow control
- ❖ Start forwarding as soon as header is received and resources (buffer, channel, etc) allocated
- ❖ Dramatic reduction in latency

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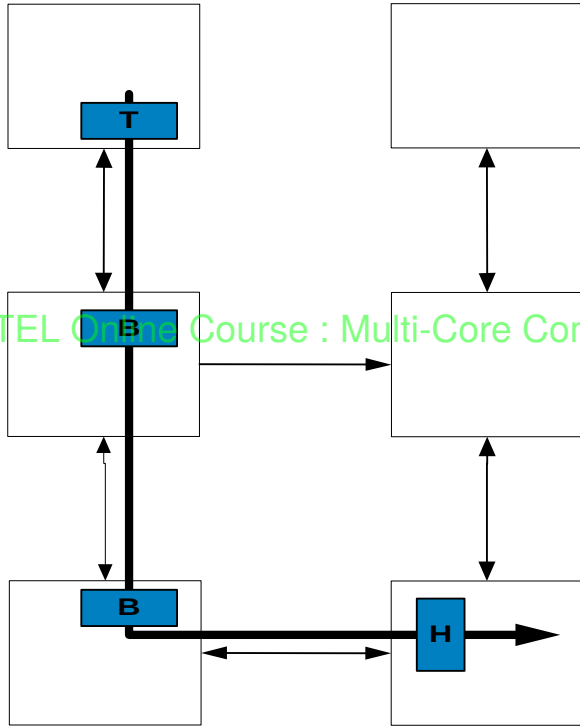


- ❖ What if packets are large?

Cut through Flow Control

- ❖ What to do if output port for head is blocked?
- ❖ Tail continue when the head is blocked, absorbing the whole message into a single switch.
- ❖ Requires a buffer large enough to hold the largest packet.
- ❖ Degenerates to store-and-forward with high contention
- ❖ Still allocate buffers and channel bandwidth for full packets

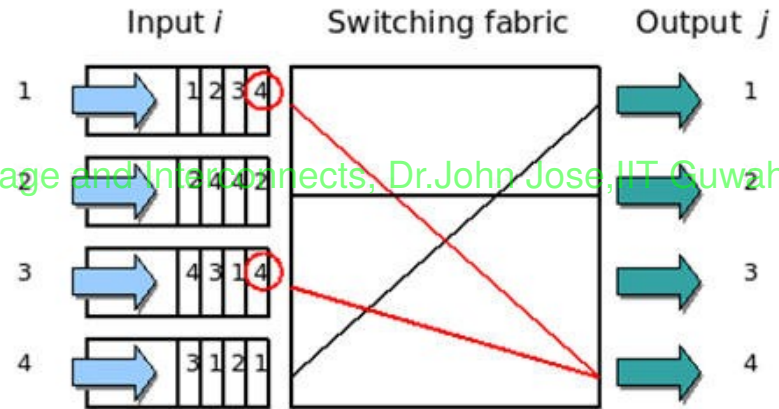
Wormhole Flow Control



- ❖ Packets broken into smaller flits
- ❖ Flits are sent across the fabric in a *wormhole fashion*
 - ❖ Body follows head, tail follows body
 - ❖ Pipelined
 - ❖ If head blocked, rest of packet stops
 - ❖ Routing (src/dest) information only in head
- ❖ Lower latency, efficient buffer utilization
- ❖ Occupies resources across multiple routers

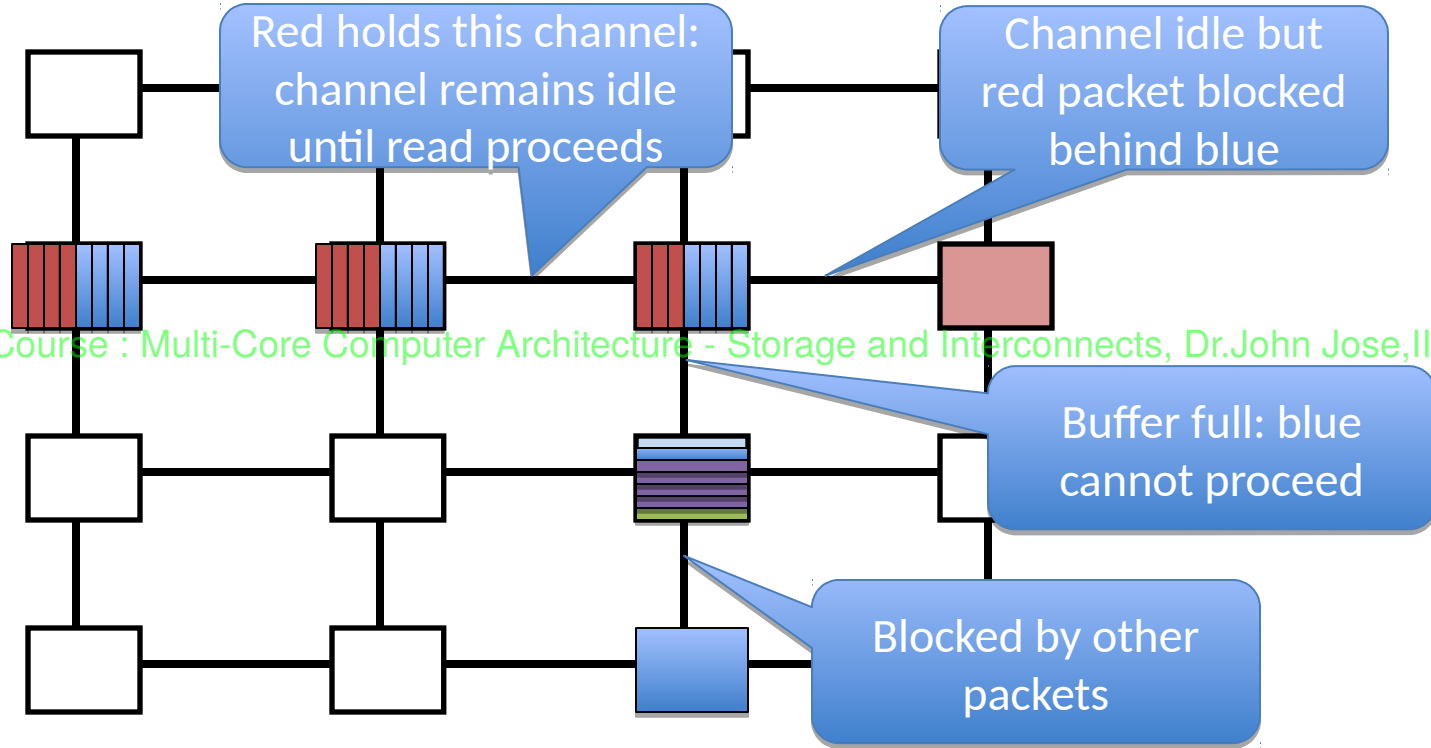
Head of Line Blocking

- ❖ Suffers from **head of line blocking**
 - ❖ If head flit cannot move due to contention, another worm cannot proceed even though links may be idle



HOL Blocking

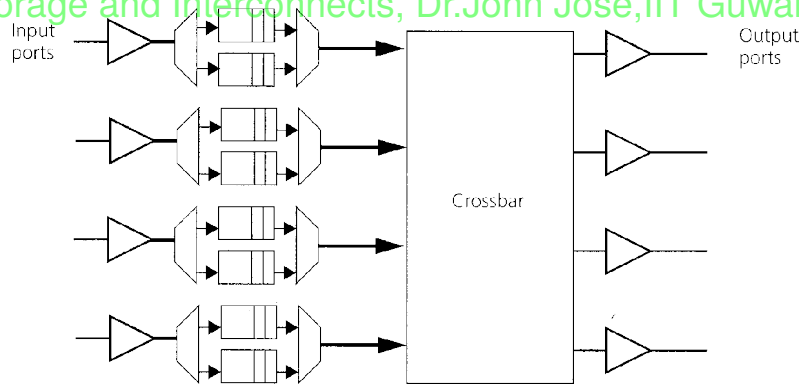
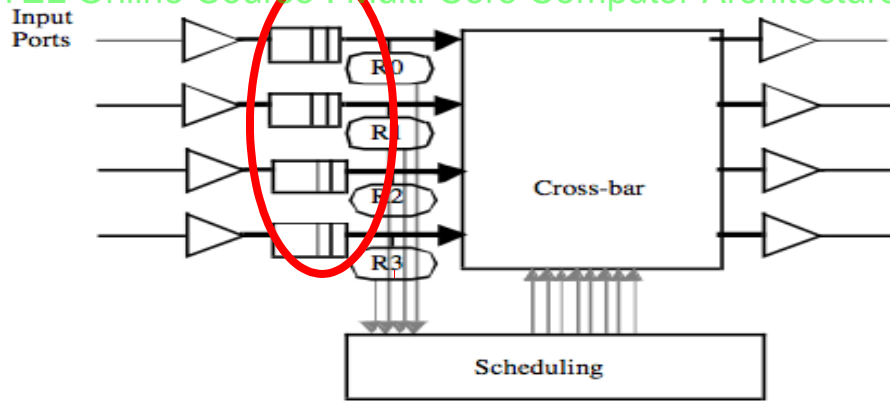
Head of Line Blocking



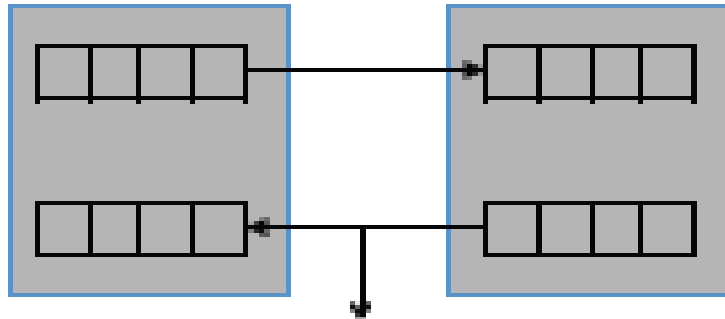
Virtual Channel Flow Control

- ❖ Multiplex multiple channels over one physical channel
- ❖ FIFO buffers replaced with multilane buffers
- ❖ Divide up the input buffer into multiple buffers sharing a single physical channel

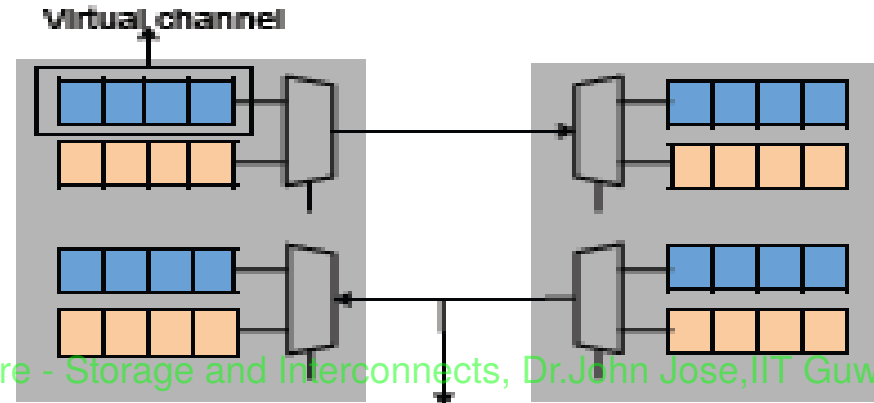
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Virtual Channel Flow Control



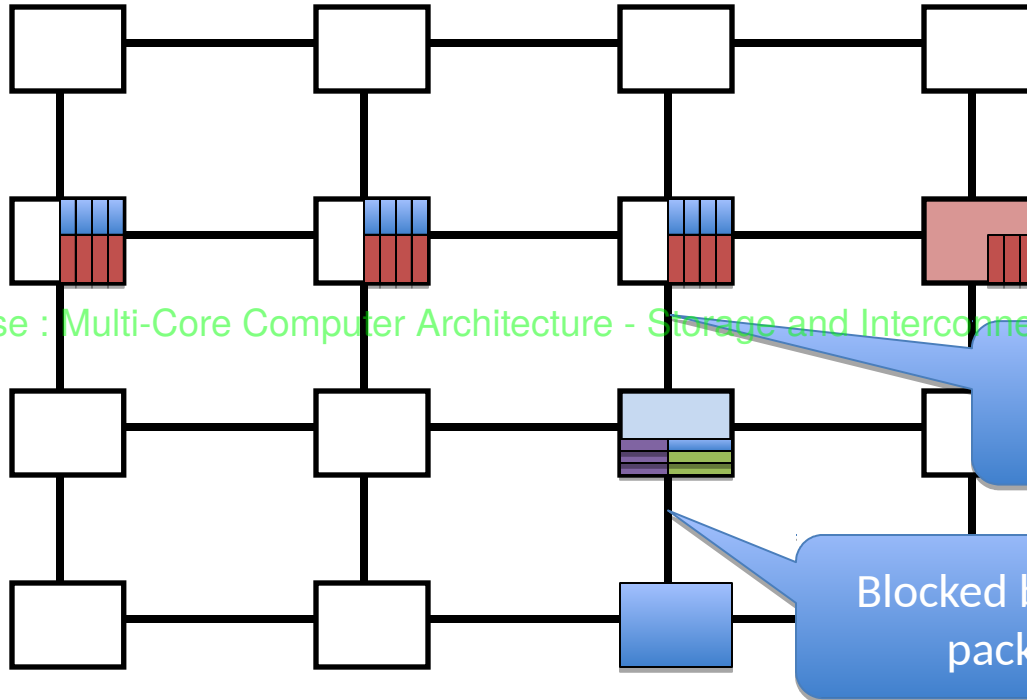
Physical channel



Physical channel

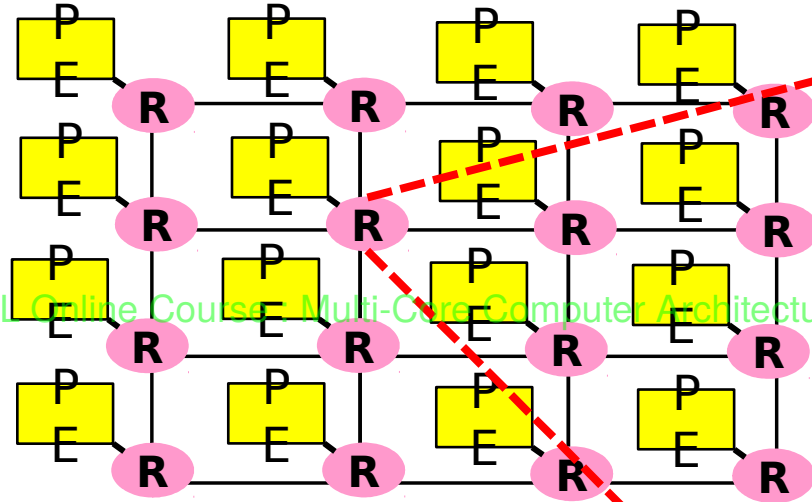
- ❖ VCs are allocated once at each router to the head flit and remaining flits of the packet inherit the same VC
- ❖ Flits of different packets can be interleaved on the same physical channel
- ❖ VCs avoid deadlocks

Virtual Channel Flow Control

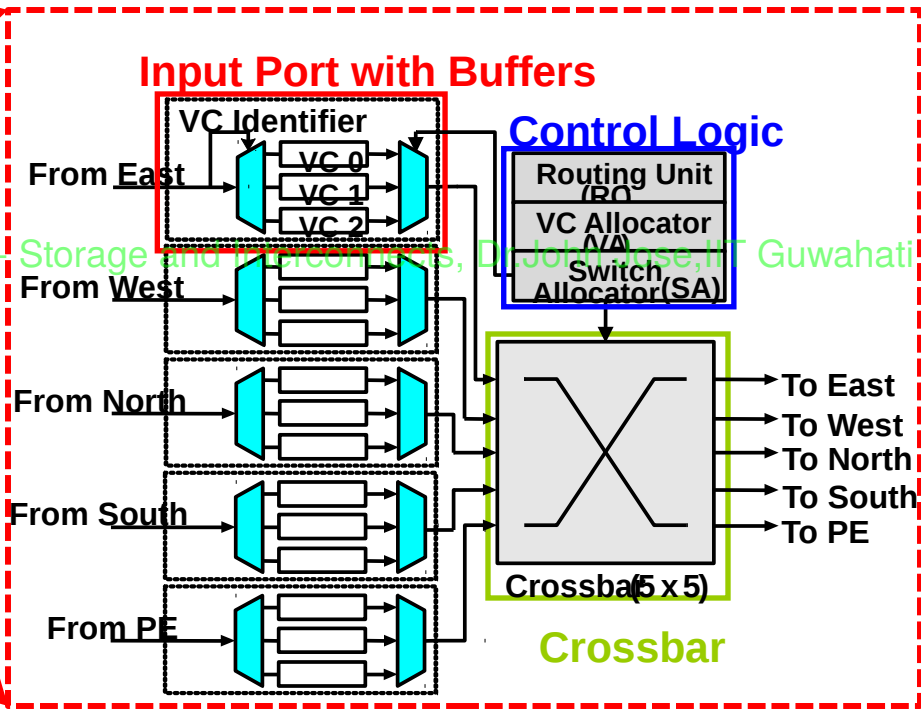


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Input Buffered NoC Router

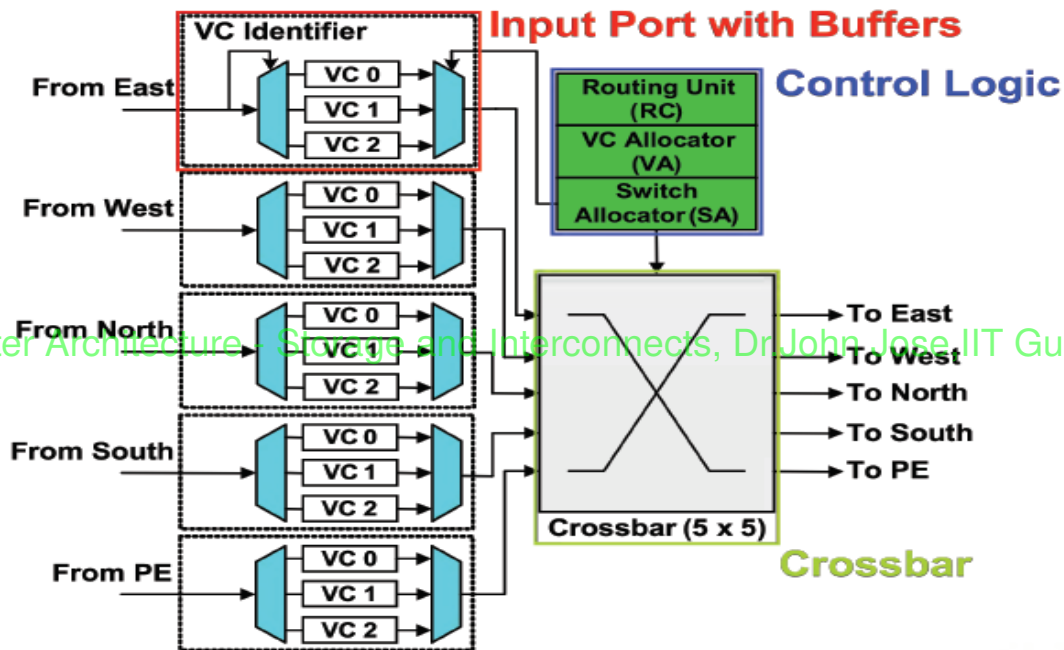


 Router
 Processing Element
 (Cores, L2 Banks, Memory Controllers etc)



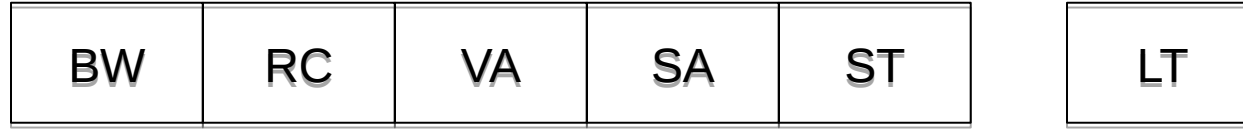
Functions of a Router

- ❖ Buffering of flits
- ❖ Route computation
- ❖ VC allocation
- ❖ Switch Allocation
- ❖ Switch Traversal
- ❖ Link Traversal



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Router Pipeline



❖ Five logical stages

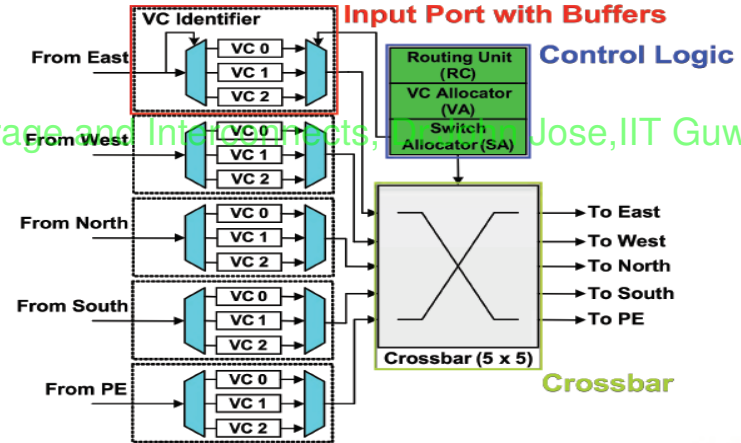
BW: Buffer Write

❖ RC: Route computation

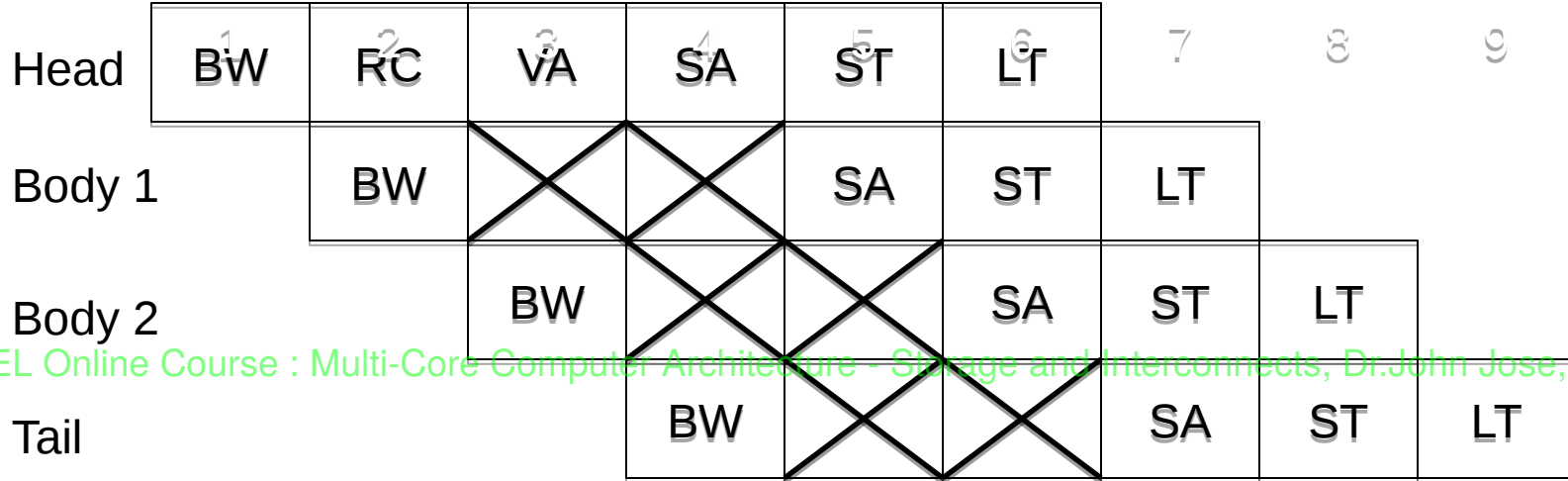
❖ VA: Virtual Channel Allocation

❖ SA: Switch Allocation

❖ ST: Switch Traversal

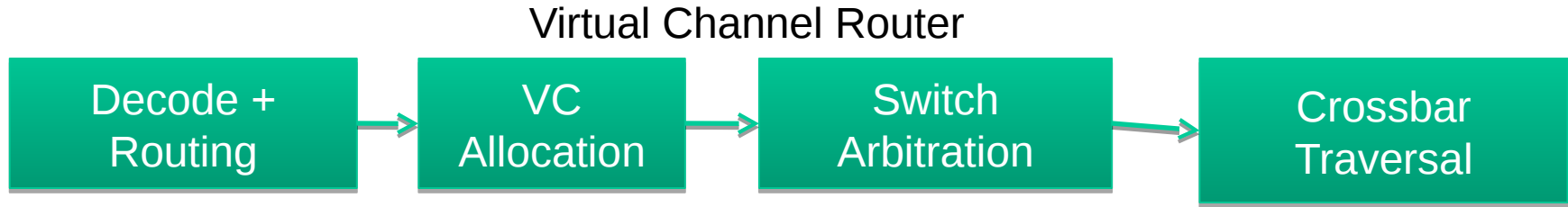


Wormhole Router Timeline



- ❖ Route computation performed once per packet
- ❖ Virtual channel allocated once per packet
- ❖ Body and tail flits inherit this information from head flit

Dependencies in a Router



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- ❖ Dependence between output of one module and input of another
 - ❖ Determine critical path through router
 - ❖ Cannot bid for switch port until routing performed

Lookahead Routing

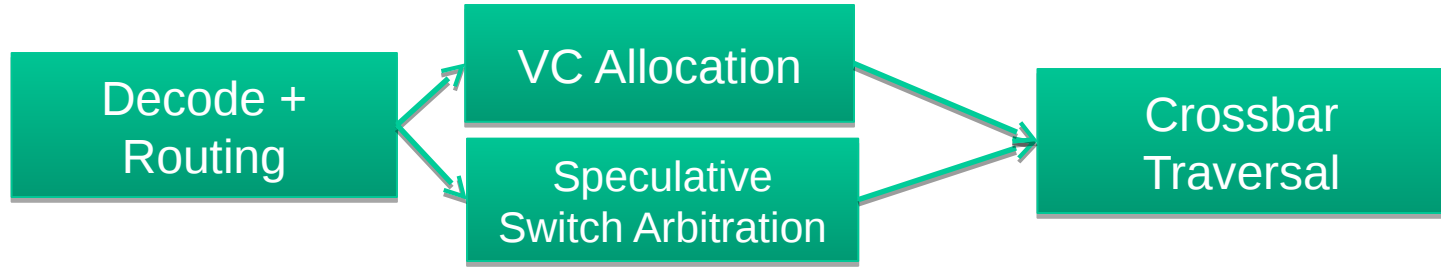
- ❖ At current router perform routing computation for next router
 - ❖ Overlap with BW

BW RC	VA	SA	ST	LT
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- ❖ Pre-computing route allows flits to compete for VCs immediately after BW
- ❖ RC decodes route header
- ❖ Routing computation needed at next hop
 - ❖ Can be computed in parallel with VA

Speculative Routing

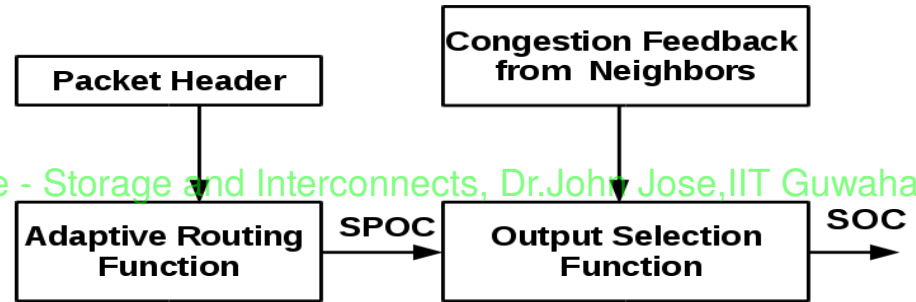
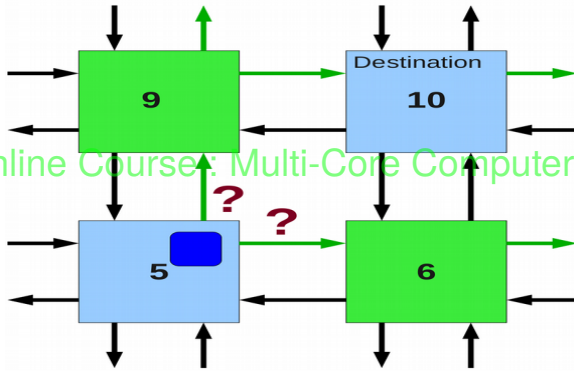


BW	VA	ST	LT
RC	SA		

- ❖ Assume that Virtual Channel Allocation stage will be successful
 - ❖ Valid under low to moderate loads
- ❖ Entire VA and SA in parallel
- ❖ If VA unsuccessful (no virtual channel returned)
 - ❖ Must repeat VA/SA in next cycle

Selection Strategy

When there are multiple possible paths for a packet at a router, which one to choose ?

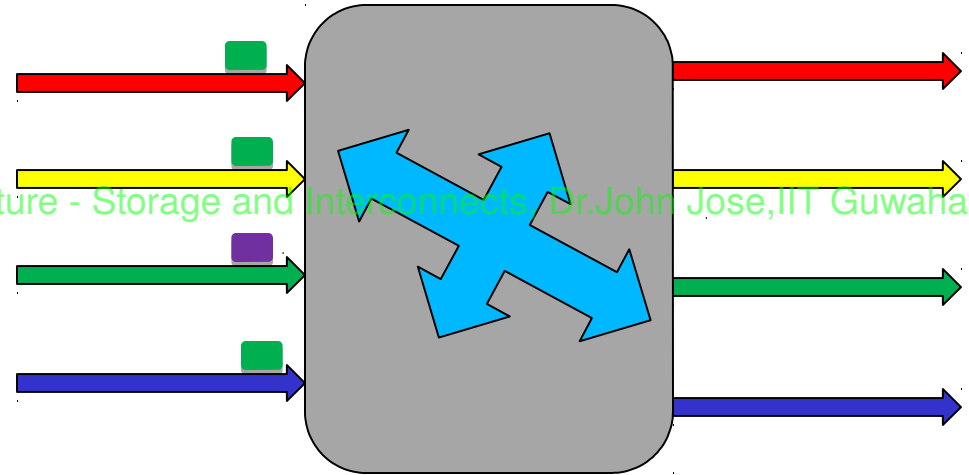
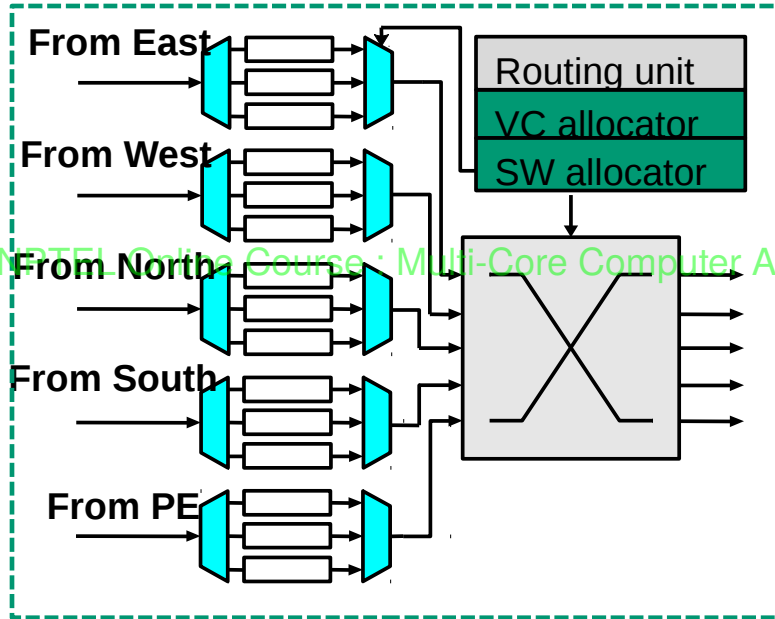


SPOC- Set of Possible Output Channels

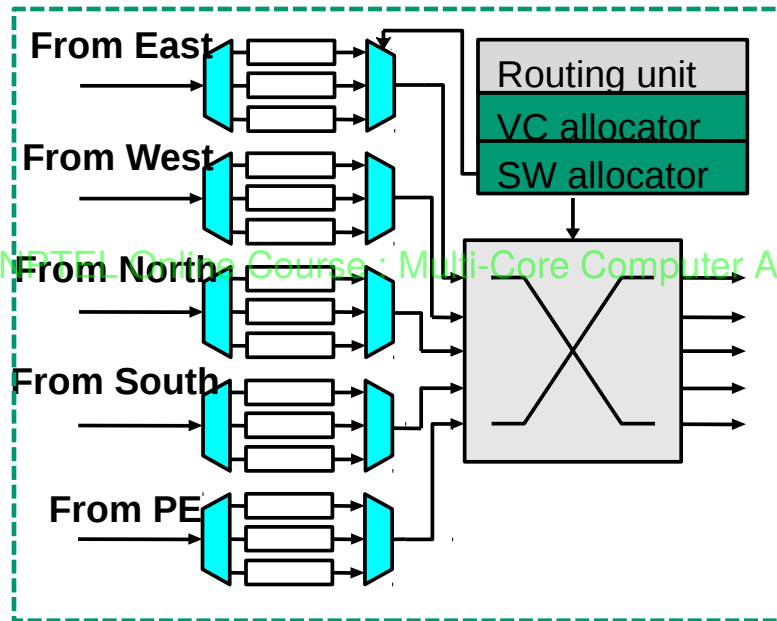
SOC- Selected Output Channel

Input / Output Channel Selection

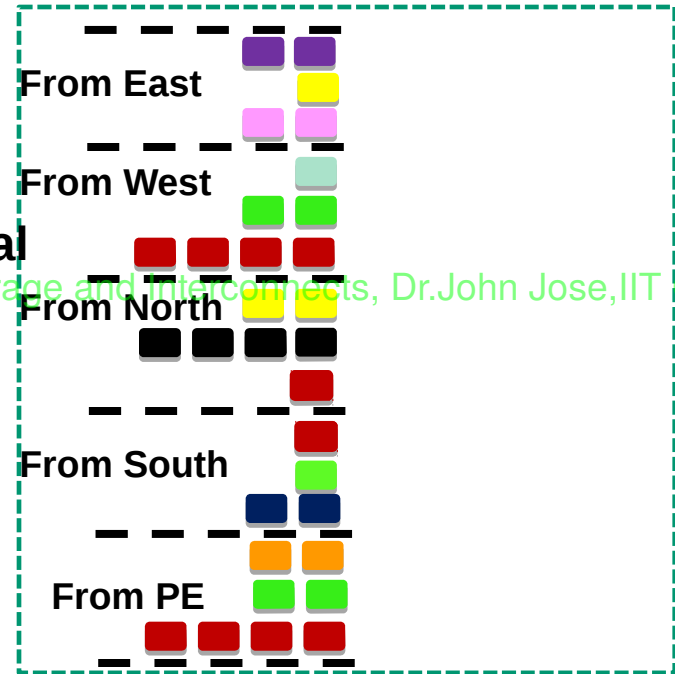
Output Channel Selection Input Channel Selection



Switch Level Packet Scheduling in NoC



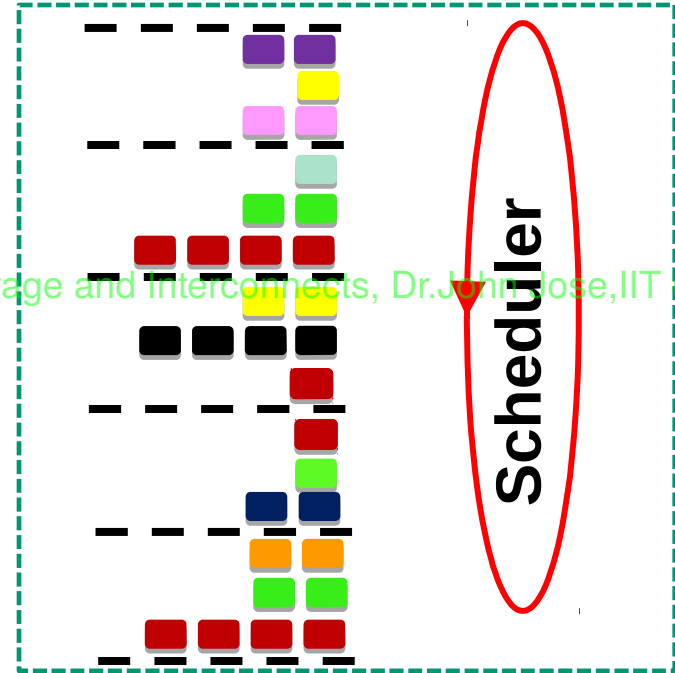
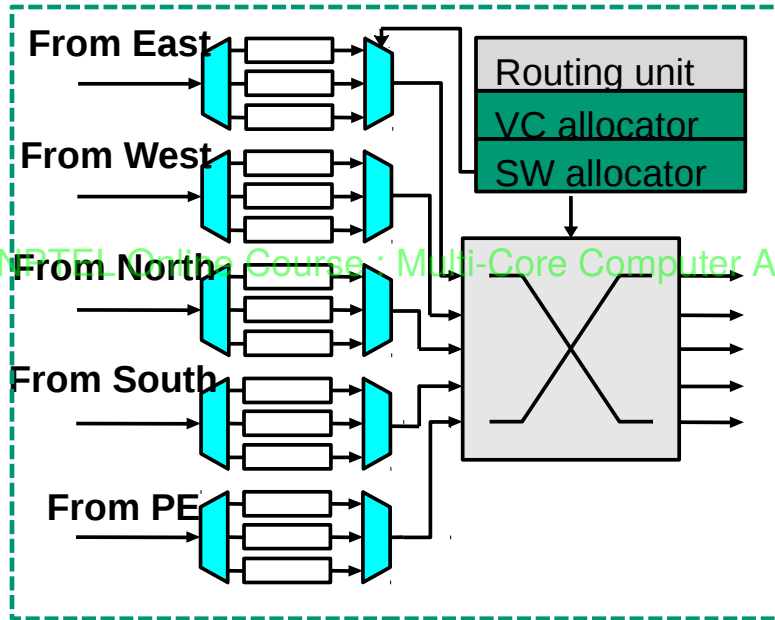
Conceptual
View



App1 App2 App3 App4
App5 App6 App7 App8

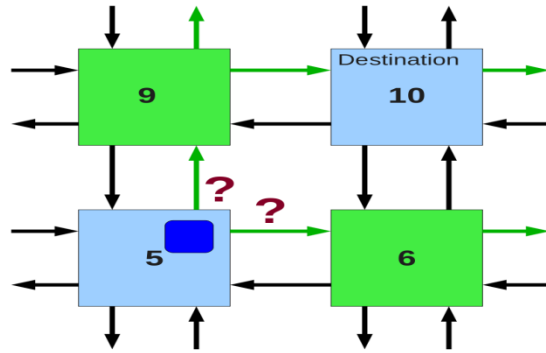
Input / Output Channel Selection

Which packet to choose?



App1 App2 App3 App4
App5 App6 App7 App8

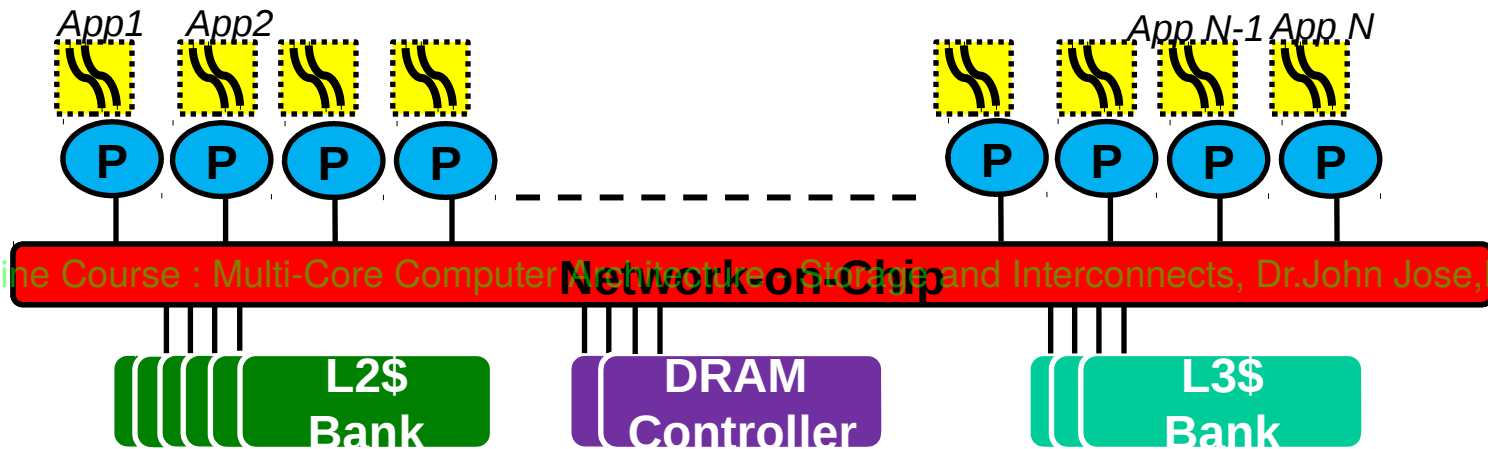
Why selection strategy important ?



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- ❖ Cache miss / coherence packets need to be serviced fast.
- ❖ To service them fast we need to reduce latency of packets.
- ❖ Congestion increases average latency of packets.
- ❖ Selection strategy chooses paths with less congestion.
- ❖ A good selection strategy reduces average packet latency.

How critical is NoC ?



Network-on-Chip is a **critical** resource
shared by **multiple applications**

**THANK
YOU!**

FOR

YOUR

PRESENCE

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